International Journal of Electrical and Electronics Research ISSN 2348-6988 (online)
Vol. 2, Issue 4, pp: (74-83), Month: October - December 2014, Available at: www.researchpublish.com

MATLAB - Based Simulation & Analysis of Nine Level NPC Multilevel Inverter Applied to Induction Machine Drive

[1]V.S R.V CHINNA RAO, [2]B. GANGA RAJU

[1]M-tech Student Scholar, Department of Electrical & Electronics Engineering, Kakinada Institute of Technology and Science, Divili, East Godavari Dt, A.P, India.
[2]Assistant Professor, Department of Electrical & Electronics Engineering, Kakinada Institute of Technology and Science, Divili, East Godavari Dt, A.P, India

Abstract: **This study presents different technologies and topologies of medium-voltage (MV) drives available on the market. The carriers above and below zero reference line are in same phase. If all the carriers are selected with the same phase, the method is known as Phase Disposition (PD) method. In this paper, four multilevel Pulse width-modulation methods; phase disposition (PD), switching-loss minimization (SLM), and selective harmonic elimination (SHE) up to the 17th and 29th harmonics, respectively, are considered. The characteristics of long-cable effects on common mode voltage (CMV) and differential-mode voltage (DMV), inverter losses and efficiency, induction machine voltage, and current harmonics are analyzed. MATLAB/Simulink for control systems are experimentally verified with a 1000-hp 4160-V neutral-point-clamped adjustable speed-drive system that includes a 24-pulse front-end voltage source converter.**

Keywords: **Harmonics, multilevel pulse width modulation, power quality, three-level neutral-point-clamped medium-voltage drives.**

I. INTRODUCTION

Due to technology advancements in semiconductor devices such as insulated gate bipolar transistors (IGBTs), modern medium voltage (MV) drives are increasingly used in petrochemical, mining, steel and metal, transportation industries among others to conserve electric energy, increase productivity and improve product quality. The development of MV drives was also motivated by the proved improvement in the efficiency, weight and volume of the motor and in the reduced installation costs in cabling, cable trays etc. One of the major markets for MV drives is retrofit applications. It is reported that 97% of the currently installed MV motors operate at a fixed speed, and only 3% of them are controlled by variable-speed drives. When fans or pumps are driven by a fixed-speed motor, the control of air or liquid flow is normally achieved by conventional mechanical methods, such as throttling control, inlet dampers, and flow control valves, resulting in a substantial amount of energy loss. The installation of the MV drive can lead to a significant savings on energy cost. It was reported that the use of the variable-speed MV drive resulted in a payback time of the investment from one to two and a half years.

Fig. 1 shows a general block diagram of an indirect MV drive. Depending on the system requirements and the type of the converters employed, the line- and motor-side filters are optional. A phase-shifting transformer with multiple secondary windings is often used mainly for the reduction of line-current distortion. The rectifier converts the utility supply voltage to a dc voltage with a fixed or adjustable magnitude. The commonly used rectifier topologies include multipulse diode or thyristor rectifiers and pulse width modulated (PWM) rectifiers. The dc filter can simply be a capacitor that provides a stiff dc voltage in voltage-source drives or an inductor that smoothes the dc current in current source drives.

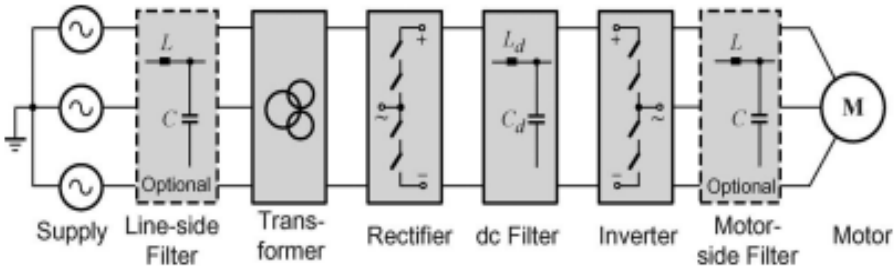

Fig. 1. General block diagram of the MV drive

Although ML-VSIs were originally developed to reach higher voltage operation, before being restricted by semiconductor limits, the extra switches and sources (provided by multiple dc-link capacitors) could be used to generate different output-voltage levels, enabling the generation of a stepped waveform with less harmonic distortion, reducing dv/dt's and common-mode voltages, and enabling operation under fault conditions and converter modularity . These characteristics have made them popular for high-power MV applications. Many topologies have been developed, among them, the neutral-point clamped (NPC) , flying capacitor (FC) , and the cascaded H-bridge (CHB) , are the most studied and commercialized by major manufacturers. MV VSDs have a semiconductor-based bridge at input. This bridge may draw distorted current that can pollute the power supply and reduce the power factor due to the harmonics components.

There are several problems for the loads connected to a polluted utility supply:

• **Capacitors:** increase in temperature, increase in losses, life time reduction, over-voltage, over current and dielectric rupture;

• **Motors:** increase in temperature, increase in noise, life time reduction, efficiency reduction, bearing and bushing damage and torque cogging;

• **Fuses / Circuit Breakers / Disconnecting Switches:** improper operation;

• **Transformers:** increase in temperature, increase in iron and copper loss and life time reduction;

• Meters: measurement errors;

• **Installation:** neutral over-heating in installations and power factor reduction;

• **Electronic Equipment:** operational fault;

• **Cables:** increase in losses caused by the higher effective current value.

There are guidelines for harmonic regulation such as the IEEE STD 519 recommendations [4]. In several low voltage applications, the 6 pulse variable frequency drive with an input line reactor or a DC reactor may perfectly meet these recommendations. When it is not enough, some techniques can be used to reduce the harmonic currents such as:

II. SYSTEMMODELING ANDDESCRIPTION

A. System Configuration

A modern three-level MV NPC ASD system, equipped with a 24-pulse transformer front end, is illustrated in Fig. 2. The three-phase ac source is fed to a three-phase 24-pulse ac-to-dc converter. The input source impedance in phase A is Lsa, along with Ra, and the line impedances are assumed to be balanced. The output dv/dt or sinusoidal filter can be used to attenuate the motor terminal over voltages caused by long cables and mitigate lower order harmonics. It is also assumed that the output filter and the induction machine (IM) load are balanced.

B. PD Modulation Method

Carrier-disposition PWM technique was first proposed in [12], with three well-known typical realizations, namely, phase disposition (PD), phase opposition disposition (POD), and alternative POD. In this paper, the PD algorithm is selected to compare with the switching-loss minimization (SLM) algorithm, as well as the SHE method. The pros and the cons of the PD, SLM, and SHE methods in the MV three-level NPC are discussed. Fig. 2 shows the modulating and carrier waveforms

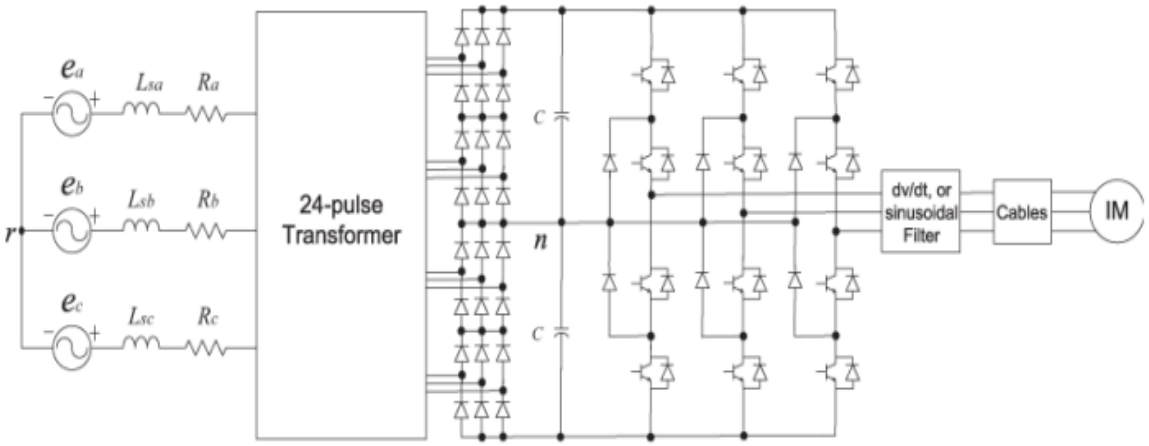

Fig. 2. Practical MV three-level NPC IM ASD system.

Technology to a well-established and attractive solution for MV high-power applications, challenges and opportunities exist in improving the load power quality, the ASD efficiency, and the common-mode voltage (CMV) rejection. Lower switching frequency becomes a necessity for reduced losses at higher power; thus, control architectures that incorporate harmonics mitigation are sought after, such as the selective harmonic elimination (SHE) method [13]. A unified approach is introduced in [13] for generating pulse width modulation (PWM) patterns in three-phase current–source rectifiers and inverters, which provides unconstrained SHE and fundamental current control. A mirror surplus harmonic method is proposed for double-cell (five levels) inverters [14]. A generalized formulation of quarter-wave symmetrical SHE problems according to the rising and falling edges of the PWM waveforms for multilevel inverters is proposed in [15] and [14]. The SHE methods for high-power MV applications are discussed in and. The technique of [12] eliminates all triplen and even harmonics, utilizes up to 100%of the dc bus voltage, and guarantees that the three-phase voltages sum up to zero at any instant. CMV issues associated with SHE based PWM are studied in [2]. In addition, the optimal PWM technique [7] is described. Both the SHE and optimal PWM concepts are reviewed in papers with low switching frequencies, but the characteristics of long-cable effects on CMV and differential-mode voltage (DMV), the tradeoffs of losses, and the output harmonics characteristics between the traditional PWM methods and the SHE have not been discussed. With modern insulated-gate bipolar transistor (IGBT) controls, the peak voltage begins to occur with a cable length of a few feet and can reach two times the controlled dc bus voltage at a length less than 50 feet. Comprehensive research in LV drives has been conducted on the modelling and the analysis of overvoltage generation on motor terminals [11]. The mitigation solutions of passive and active electromagnetic-interference filters are proposed [15]. Very little has been published to date regarding the quantitative characteristic analysis comparing multilevel PWM methods in MV high-power industrial ac drives. In this paper, several key indexes of MV drive characteristics on power-quality and design issues are evaluated through analysis, simulation, and experiments of a 1000-hp 4160-V NPC based ASD system. Performance comparisons of pros and cons on various PWM methods are provided to aid design selections and applications for practicing engineers.

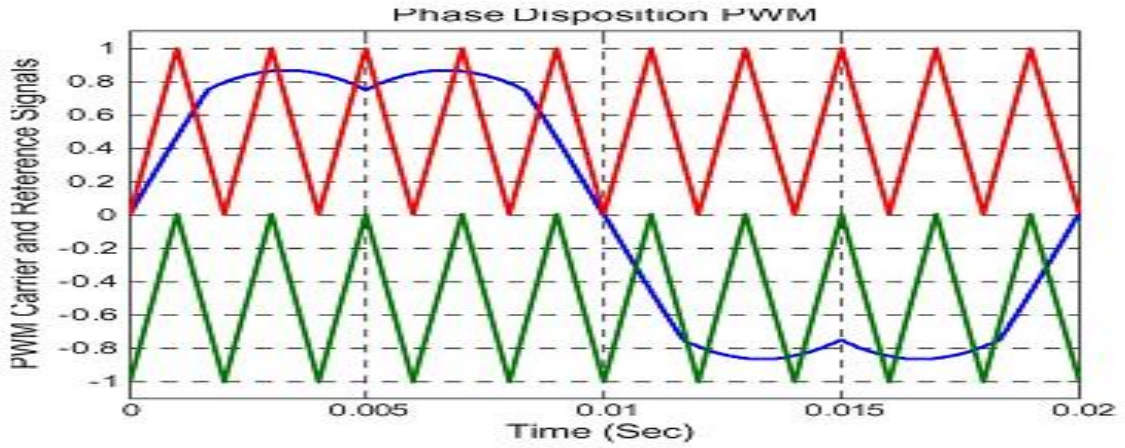

Fig. 3. PD PWM scheme. (Red and green) Carrier signals. (Blue) Reference signal.

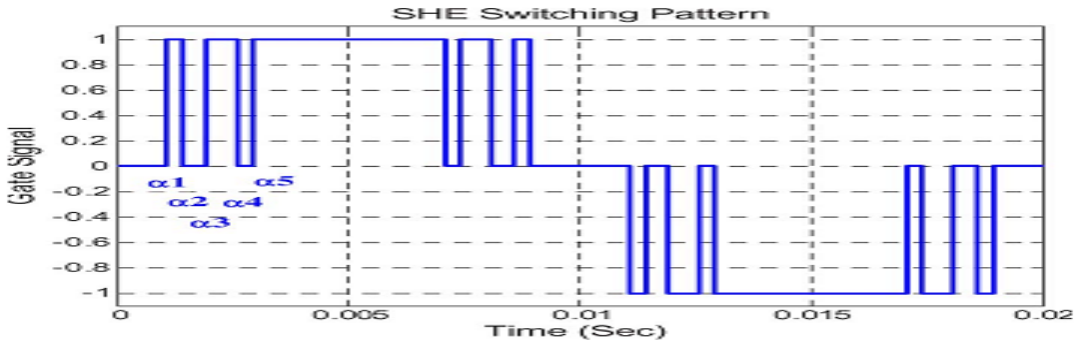

Fig. 4. SHE PWM scheme with up to 13th-harmonic removal.

Of phase A for a three-level NPC inverter in the PD mode. In industrial applications, the PD-based PWM is commonly adopted.

C. SHE Modulation Method

Fig. 4 demonstrates the SHE example with five angles to remove up to the 13th harmonic. The voltage level changes at anglesα1...α5. From the Dirich let theorem, the pulse can be expressed in Fourier series, i.e.,

$$V(t) = \frac{a_0}{2} + \sum_{1}^{\infty}(a_n \cos nax + b_n \sin nax)$$

Where

$$a_n = \frac{2}{T}\int_{\frac{-T}{2}}^{\frac{T}{2}} v(t)\cos nax\, dt$$

$$b_n = \frac{2}{T}\int_{}^{\frac{T}{2}} v(t)\sin nax\, dt. \qquad (1)$$

Due to the nature of the quarter-wave symmetry, an=0, and unreduced to

$$\frac{2E}{n\pi}\sum_{k=1}^{n}[(-1)^{k+1}\cos na_k + (-1)^k \cos(n\pi - na_k)]$$

$$b_n = \frac{4E}{n\pi}\sum_{k=1}^{n}(-1)^{k+1}\cos na_k,\ n = 1,3,5\ldots. \qquad (2)$$

Equation (2) allows the angles be calculated to eliminate certain harmonics in the system. If the number of pulses or angles is kept low, the IGBT switching losses are reduced.

D. SLM Modulation Method

In high-power MV drives application, the switching frequency is often limited below 1 kHz. The output current harmonics can be fairly high. The SLM PWM scheme can allow the system to operate at a relatively higher switching frequency

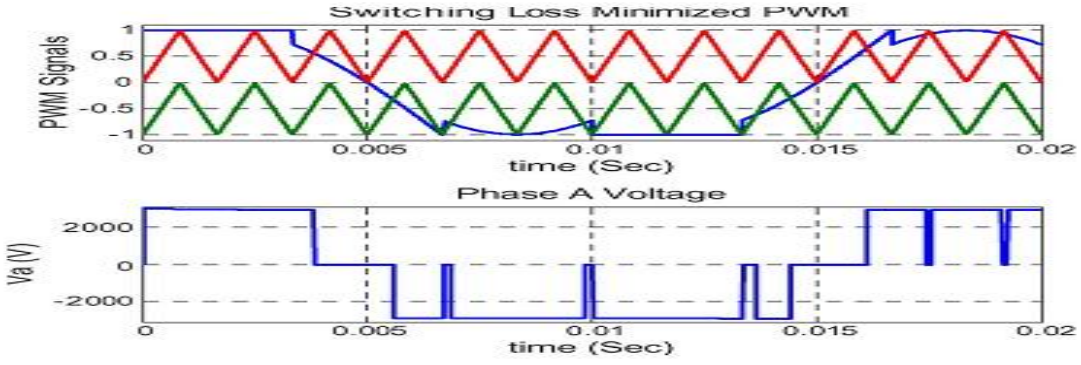

Fig. 5. SLM PWM scheme. (Top) Red and green are carrier signals, and blue is the reference signal. (Bottom) Resulting phase-A voltage.

While reducing the inverter total power losses. This may be approximately determined as a function of switching time, i.e., the instantaneous value of the current and the voltage at the switching time. Switching loss Psw in the IGBT device can be approximately expressed as [10]

$$P_{\text{sw}} = \frac{\sum_{j=1}^{n} \frac{1}{6} v_j i_j (T_{\text{on}} - T_{\text{off}})}{T} \quad (3)$$

Where,

T inverter output period of the fundamental component;

Ton turn-on time;

Toff turn-off time;

N total number of the switching cycles in one period T;

J j^{th} switching event;

v_j and i_j instantaneous values of the voltage and the current at jth switching event.

From (3), it is shown that the switching loss can be improved by decreasing the switching frequency or by reducing the instantaneous value of the current or the voltage at the switching time. For the purpose of reducing the switching loss, the SLM PWM can be characterized below.

1) Stop switching for some duration within T.

2) Set the "no switching" duration in the center of the peak value region of the current.

Fig. 5 shows the modulating and carrier waveforms of one phase in the SLM PWM scheme.

E. Long-Cable IM Models

In applications where the cable length is long, the motor terminals' voltage $V_m=V_{inv}+V_{rev}$, where V_{inv} is the inverter output voltage and V_{rev} is the reflected voltage portion on the motor terminal. Each term is defined as

$$V_{\text{rev}} = \frac{Z_L - Z_C}{Z_L + Z_C} V_{\text{inv}} \quad (4)$$

$$V_m = V_{\text{inv}} + V_{\text{rev}} = \frac{2 Z_L}{Z_L + Z_C} V_{\text{inv}} \quad (5)$$

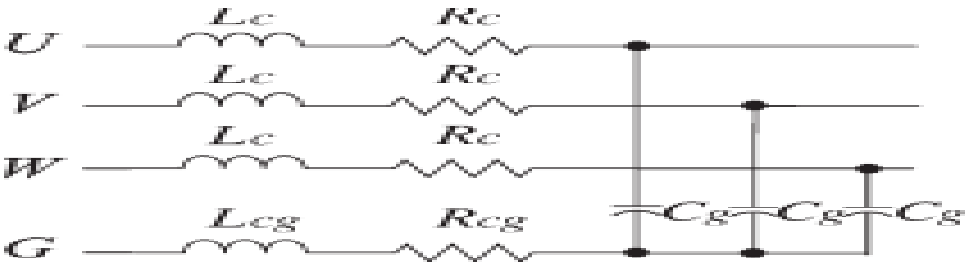

Fig. 6. Per-unit-length distributed cable model

TABLE 1. Load cable parameters

L_c	R_c	C_g	L_{cg}	R_{cg}
0.282 mH/km	0.0754 Ω/km	0.456 μF/km	0.155 mH/km	0.02735 Ω/km

TABLE 2. IM Parameters

R_s	R_r	L_{ls}	L_{lr}	L_m
95.7mΩ	100mΩ	5.32mH	5.10mH	151mH

Where Zc is the cable characteristic impedance and ZL is the motor end impedance. Typically, Vrev =(0.6~0.9)·Vinv. In order to evaluate the MV long-cable effects on the motor terminals' over voltages, the cables are modelled as the cascaded lossy distributed parameter network per unit length in Fig. 6. The cable is a 500-kcmil-American-wire-gauge 6/10-kV cross linked-polyethylene-insulated copper conductor with polyvinyl chloride jacket. The cable parameters per unit length at 20◦C are presented in Table I. The 1000-hp (746-kW) 4160-V four-pole 60-Hz IM parameters are given in Table II.

III. MATLAB MODELING AND SIMULATION RESULTS

Here simulation is carried out in two different conditions, in that 1. Three Level NPC Multilevel Converter with different modulation methods 2. Nine Level NPC Multilevel Converter with Induction Machine Drive Application.

Case 1: Three Level NPC Multilevel Converter with different modulation methods

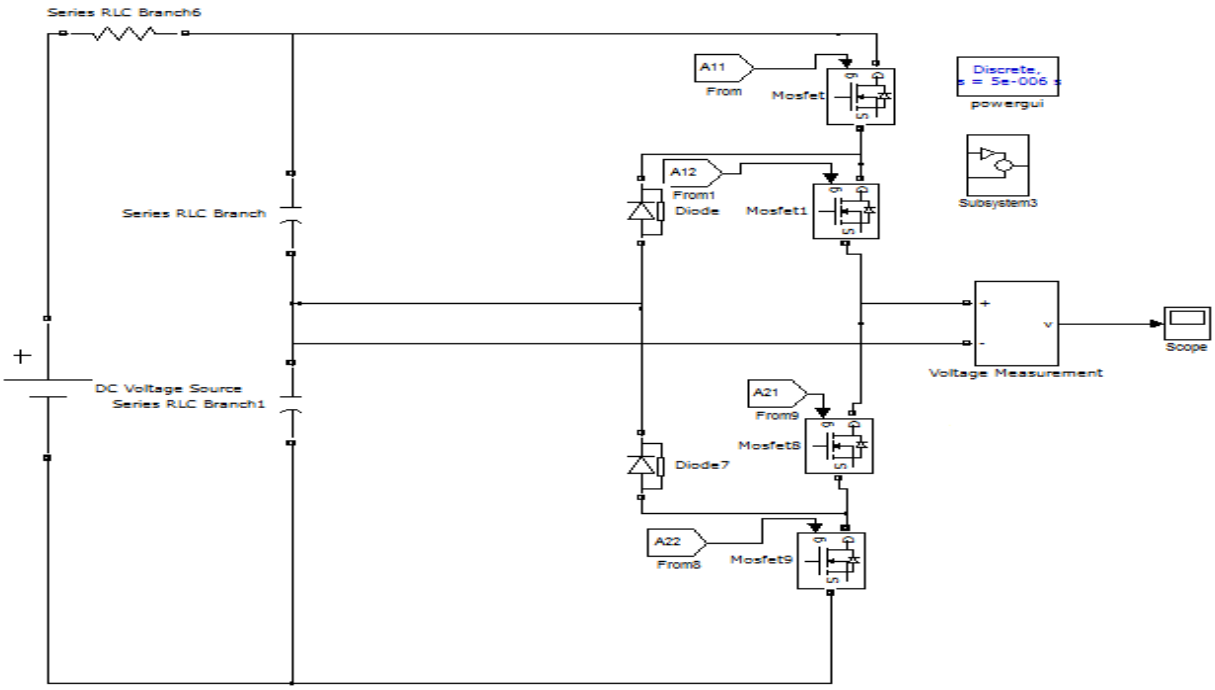

Fig.7 Matlab/Simulink Model of Proposed Three Level NPC Multilevel Converter

Fig.7 shows the Matlab/Simulink Model of Proposed Three Level NPC Multilevel Converter using Matlab/Simulink Platform.

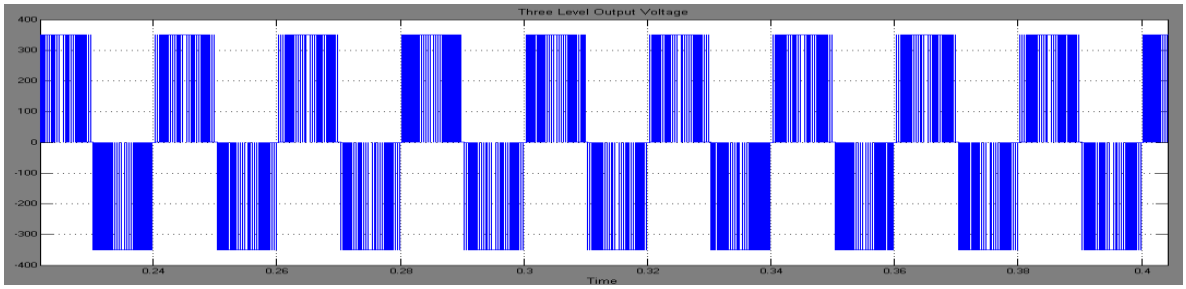

Fig.8 Three Level Output Voltage of NPC Multilevel Converter using PD Modulation Technique

Fig.8 shows the Three Level Output Voltage of NPC Multilevel Converter using PD Modulation Technique.

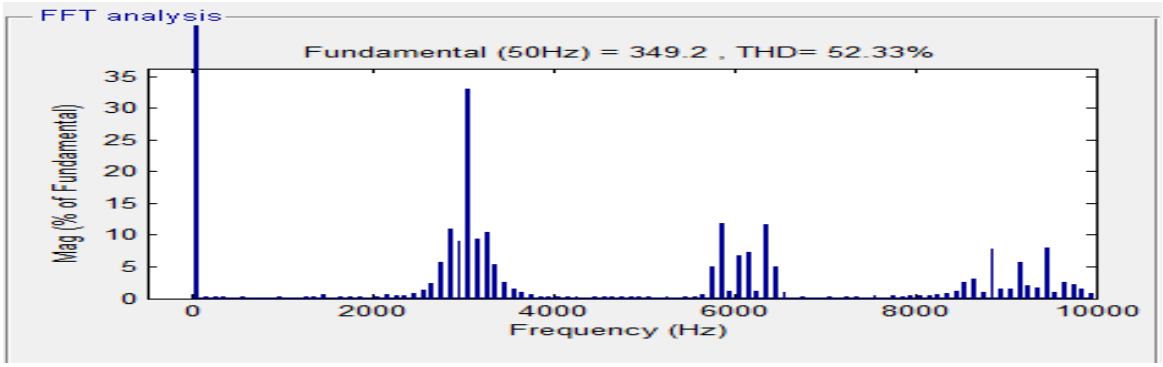

Fig.9 FFT Analysis of Three Level Output Voltage of NPC Multilevel Converter using PD Modulation Technique

Fig.9 shows the FFT Analysis of Three Level Output Voltage of NPC Multilevel Converter using PD Modulation Technique, we get 52.33%.

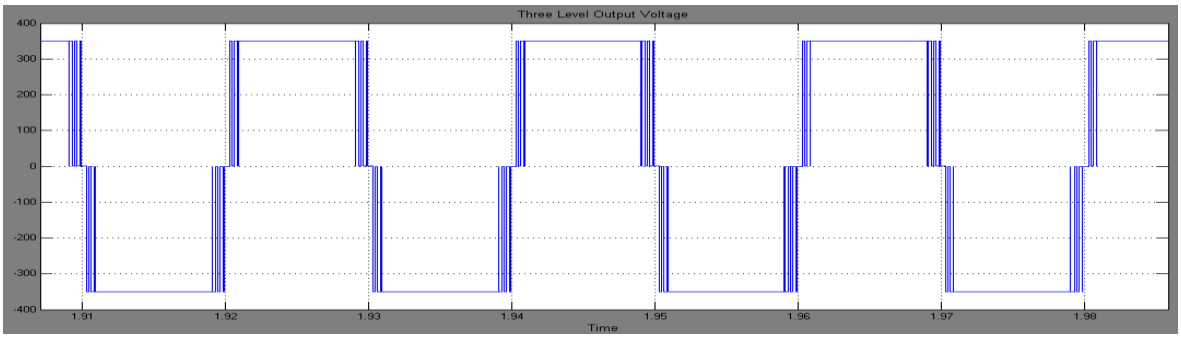

Fig.10 Three Level Output Voltage of NPC Multilevel Converter using Switching Loss Minimizing Technique
Fig.10 shows the Three Level Output Voltage of NPC Multilevel Converter using Switching Loss Minimizing Technique.

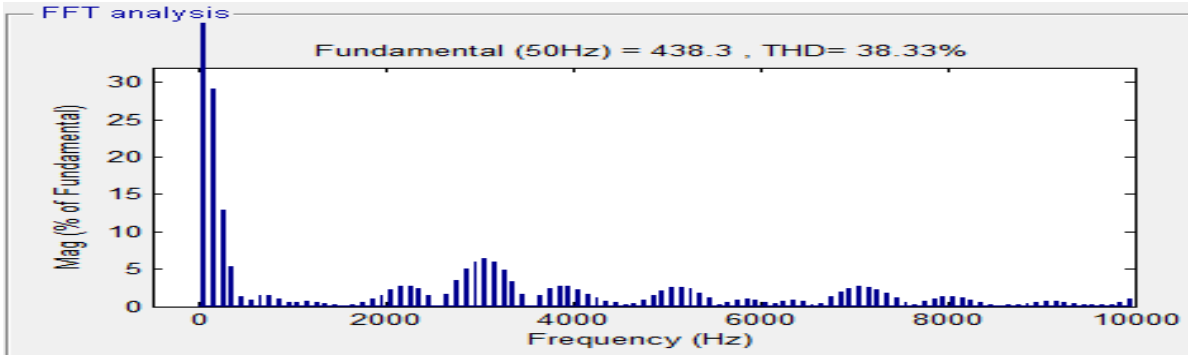

Fig.11 FFT Analysis of Three Level Output Voltage of NPC Multilevel Converter using Switching Loss Minimizing Technique

Fig.11 shows the FFT Analysis of Three Level Output Voltage of NPC Multilevel Converter using Switching Loss Minimizing Technique., we get 38.33%.

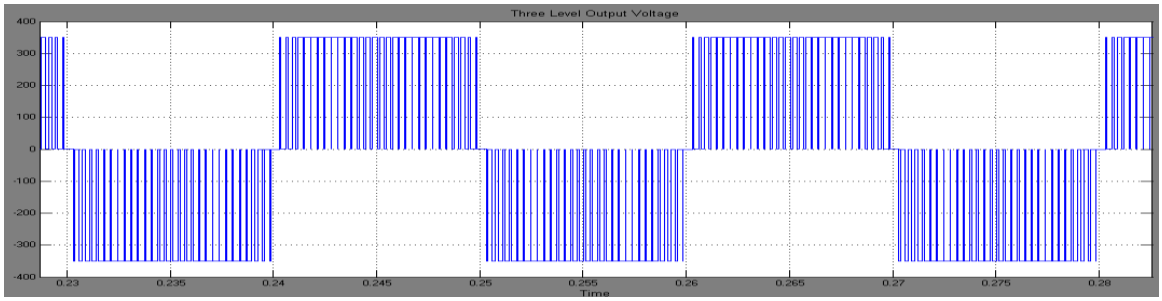

Fig.12 Three Level Output Voltage of NPC Multilevel Converter using Specific Harmonic Elimination (SHE) Technique

Fig.12 shows the Three Level Output Voltage of NPC Multilevel Converter using Specific Harmonic Elimination (SHE) Technique.

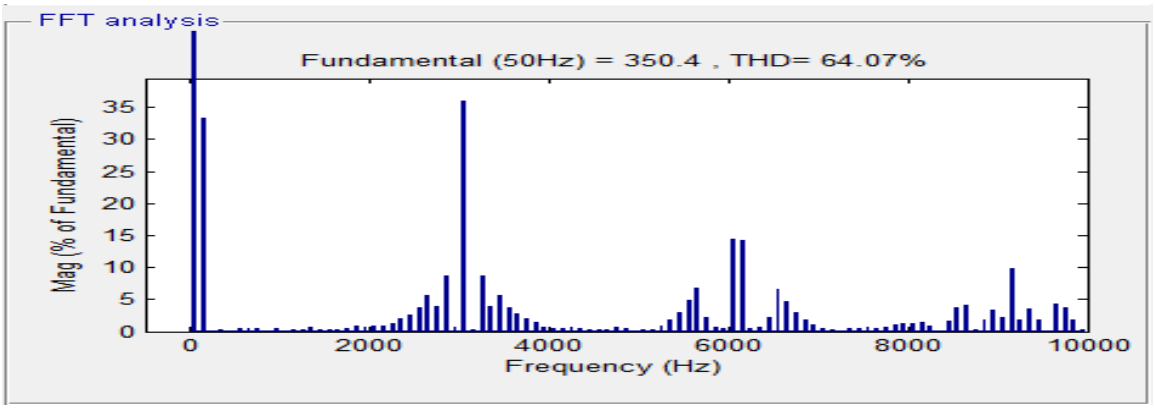

Fig.13 FFT Analysis of Three Level Output Voltage of NPC Multilevel Converter using Specific Harmonic Elimination (SHE)Technique

Fig.13 shows the FFT Analysis of Three Level Output Voltage of NPC Multilevel Converter using Specific Harmonic Elimination (SHE) Technique, we get 64.07%.

Case 1: Implementation of Proposed Concept using Neutral Clamped Type Multilevel Inverter.

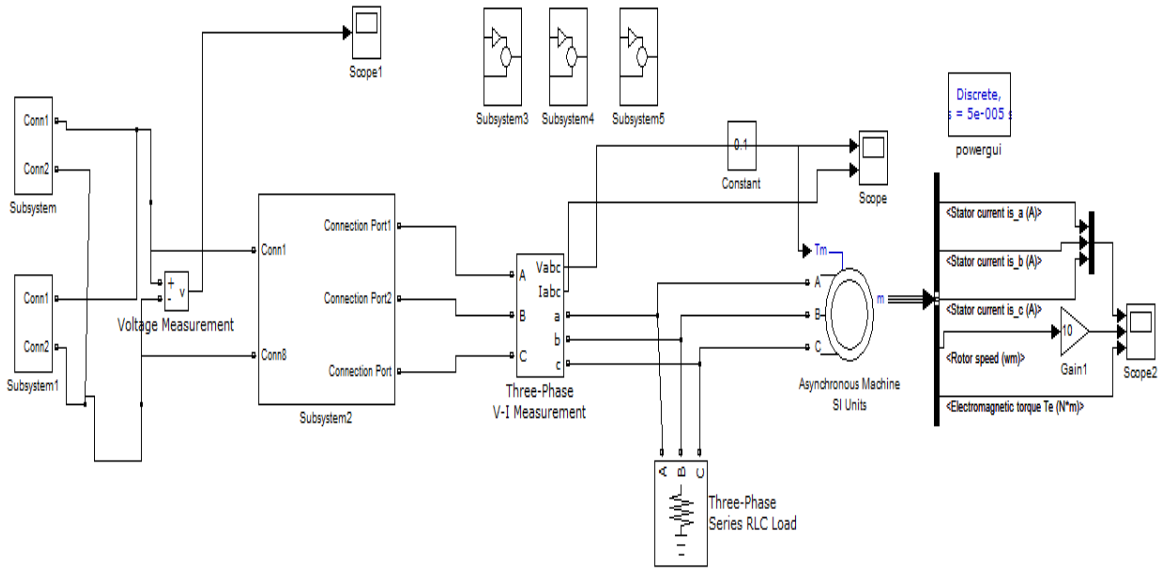

Fig. 14 Matlab/Simulink Model of Proposed NPC Converter with Induction Machine Drive

Fig.14 shows the Matlab/Simulink Model of Proposed NPC Converter with Induction Machine Drive.

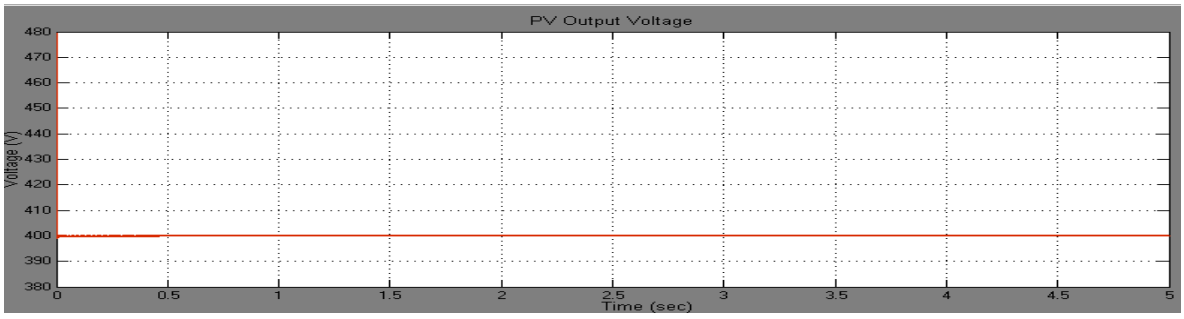

Fig.15 PV Output Voltage

Fig.15 Output Voltage coming from PV arrays with the help of high step up DC/DC Converter and directly fed to our proposed inverter.

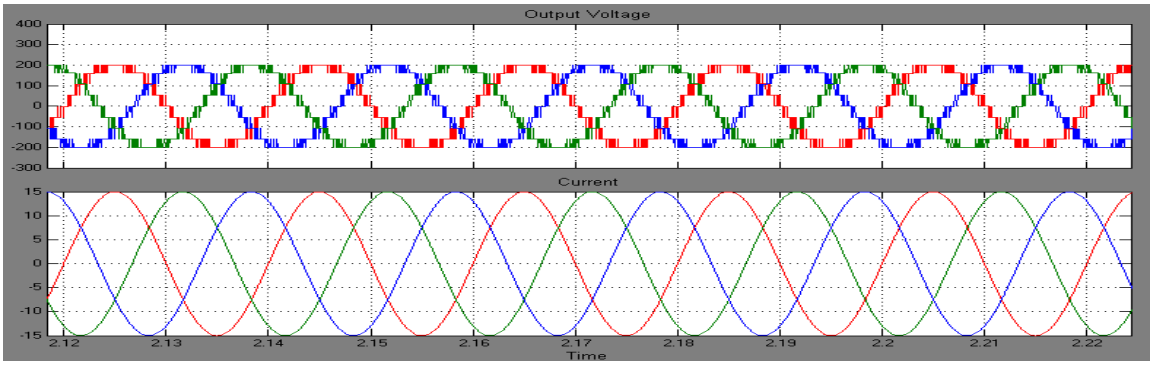

Fig.16 Level Output Voltage and Current

Fig. 16 shows the 9-Level Output Voltage and current coming from the proposed NPC multilevel inverter.

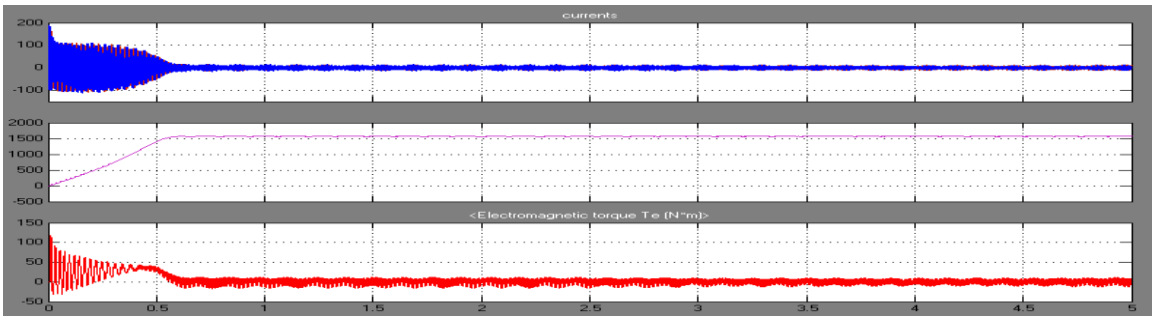

Fig.17 Stator Currents, Speed, Electromagnetic Torque

Fig.17 shows the Stator Currents, Speed, and Electromagnetic Torque of the proposed NPC Strategy Controlled Drive Performance Characteristics.

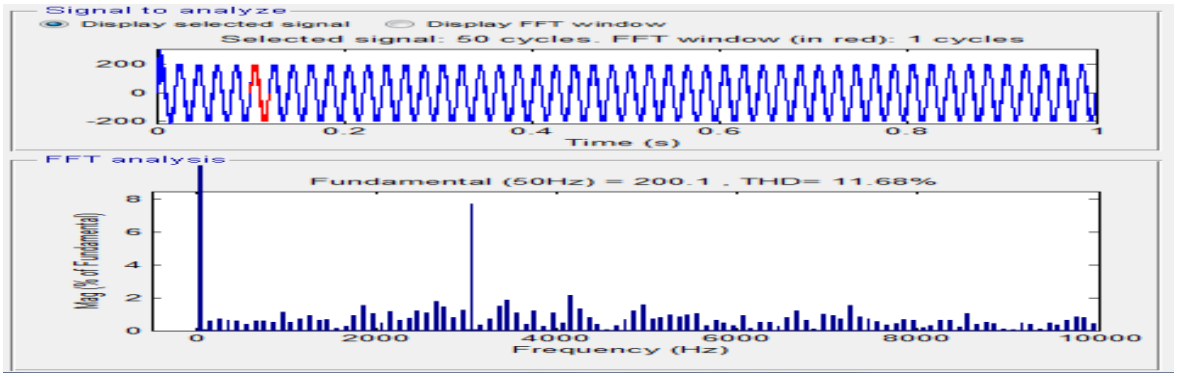

Fig. 18 FFT Analysis of Proposed NPC Converter Output Voltage

Fig. 18 shows the FFT Analysis of Proposed NPC Converter Output Voltage, we get 15.18% no need of any filter we get this value.

IV. CONCLUSION

With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic semiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices.In this paper, the quantitative power-quality and characteristic analysis of three-level PWM methods in MV high power industrial ac drives has been presented. The comparisons have involved the PD, SLM, and SHE algorithms. The Simulink models of the SHE, the SLM, and the long cable have been presented for evaluating CMV at the IM terminals, the output voltage, the current-waveform harmonic power qualities, and the inverter losses and efficiency as a function of loads (25%–100%) and output

frequency (15–60 Hz). The basic structure and operating characteristics of NPC multilevel inverter have been changed by using different pwm techniques. The inverter cell is low means the design of the inverter switch pattern is easiest. Multilevel inverter is to obtain a high resolution. The technique is used to improve the level of the inverter and extends the design flexibility and reduces the harmonics. A SPWM approach was presented to deal with the uneven power transferring characteristics of the conventional SPWM modulation techniques.

REFERENCES

[1] F. J. Bartos, "Why choose medium-voltage drives?"Control Eng. Mag.,Dec.2010.[Online].Available: http://www.controleng.com/indexphp?id=483&cHash=081010&tx_ttnews[tt_news]=36225

[2] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications,"IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[3] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," Proc. IEEE, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.

[4] Y. Shakweh and E. A. Lewis, "Assessment of medium voltage PWM VSI topologies for multi-megawatt variable speed drive applications," inProc. 30th Annu. IEEE PESC, 1999, vol. 2, pp. 965–971.

[5] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[6] J. A. Alves, G. da Cunha, and P. Torri, "Medium voltage industrial variable speed drives," WEG Appl. Note, WEG AUTOMAÇÃO, Brazil, 2010.

[7] D. Krug, S. Bernet, S. S. Fazel, K. Jalili, and M. Malinowski, "Comparison of 2.3-kV medium-voltage multilevel converters for industrial medium-voltage drives,"IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2979–2992, Dec. 2007.

[8] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter,"IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[9] K.N.V Prasad, G.Ranjith Kumar, T. Vamsee Kiran, G.Satyanarayana., "Comparison of different topologies of cascaded H-Bridge multilevel inverter," Computer Communication and Informatics (ICCCI), 2013 International Conference on , vol., no., pp.1,6, 4-6 Jan. 2013.

[10] B. P. Schmitt and R. Sommer, "Retrofit of fixed speed induction motors with medium voltage drive converters using NPC three-level inverter high-voltage IGBT based topology," inProc. IEEE ISIE, 2001, vol. 2, pp. 746–751.

[11] A. VanderMeulen and J. Maurin, "The reliability of neutral point clamped vs. cascaded H-bridge inverters," Eaton White Paper TD02000001E, Arden, NC, 2009.

[12] A. Newton and M. Sumner, "Neutral point control for multi-level inverters: Theory, design, and operational limitations," inProc. IEEE Ind. Appl. Soc. Conf., New Orleans, LA, 1997, pp. 1136–1343.

[13] J. R. Espinoza, G. Joos, J. I. Guzman, L. Moran, and R. P. Burgos, "Selective harmonic elimination and current/voltage control in current/voltage source topologies: A unified approach," IEEE Trans. Ind. Electron., vol. 48, no. 1, pp. 71–81, Feb. 2001.

[14] L. Li, D. Czarkowski, Y. Liu, and P. Pillay, "Multilevel selective harmonic elimination PWM techniques in series-connected voltage inverters," IEEE Trans. Ind. Appl., vol. 36, no. 1, pp. 160–170, Jan./Feb. 2000.

[15] W. Fei, Y. Zhang, and X. Ruan, "Solving the SHEPWM nonlinear equations for three-level voltage inverters based on computed initial values," inProc. IEEE APEC, 2007, pp. 1084–1088